LLCFR01 - LOW LATENCY CREST FACTOR REDUCTION

OVERVIEW

Crest Factor Reduction (CFR) is a key component in modern digital amplifier and linearization systems. Using active control of transmit signal Error Vector Magnitude (EVM), Crest Factor Reduction can significantly reduce waveform peak to average power ratio (PAPR), while maintaining spectral purity and improving amplifier linearity, efficiency and cost.

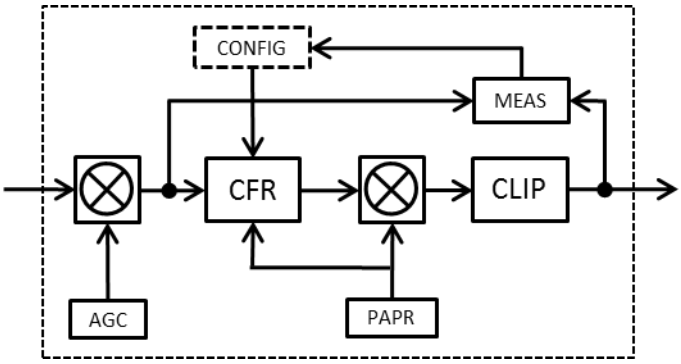
The Affarii LLCFR01 processor is an advanced non-linear cancellation engine that offers low implementation resource and power consumption. The CFR processor is modulation agnostic, supporting single and multi-carrier configurations, and can self-training without knowledge of system configuration.

The LLCFR01 core is designed support peak reduction down to 6dB PAPR dependent on modulation scheme and been qualified for operation with 3GPP WCDMA and LTE standards and with DVB-T/T2 and DAB Broadcast Standards.

FEATURES

- Multi-stage Peak Cancellation.
- Reduction to 6.0dB PAPR.
- Input Modulation Agnostic.
- MCPA Waveform Support.
- Self-Training Algorithm (optional).
- Typical Performance:
  - WCDMA: 6.5dB PAPR @ <6% EVM.
  - LTE: 7.0dB PAPR @ <4% EVM.
  - DVB-T: 8.0dB PAPR @ <-32dB MER.
- ACP1 >70dBc @ 6.0db PAPR Output.

BLOCK DIAGRAM



DESCRIPTION

The LLCFR01 Crest Factor Reduction processor is a modulation independent *h*ybrid Peak Cancellation (*h*PC-CFR) architecture based on dynamic filter technology.

For modulator and radio head applications the CFR core supports direct I+Q signal input from the modulator or multi-carrier mixer output with PAPR up to 24dB peak levels with an 18bit datapath.

The core supports up to four cascaded peak reduction stages with an input pre-scaling and output post-scaling gain elements and optional hard clip. The inclusion of scaling elements allows output signals to be peak reduced and optimally scaled to match a final 12-16bit transmit signal datapath.

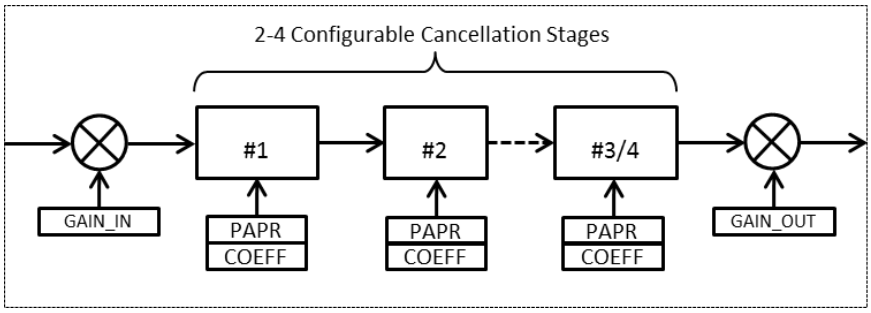


Figure 1: Multi-stage CFR Architecture

The LLCFR01 core also supports a direct IF mode for input and output data for application in delay critical RF repeater applications. Support for direct IF signals removes the requirement for IF to complex baseband (CBB) conversion with its associated resource requirement delay.

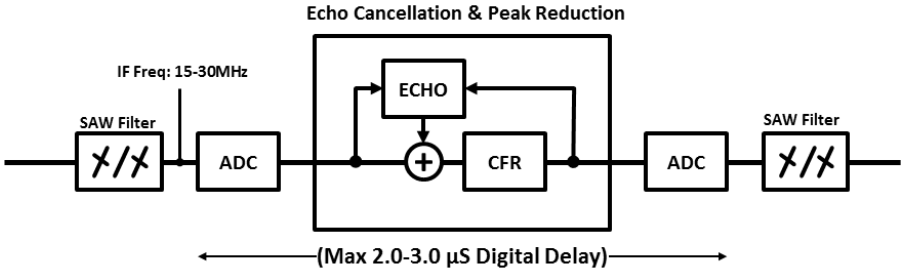


Figure 2: Low - Latency Digital Repeater with Echo and Peak Cancellation

The LLCFR01 core employs a multiplier optimised architecture which is suitable for implementation in low cost FPGA fabrics and allows full configuration of the number of reduction stages, spectral shaping length, and filter lengths to minimise overall resource and system latency for specific application requirements.

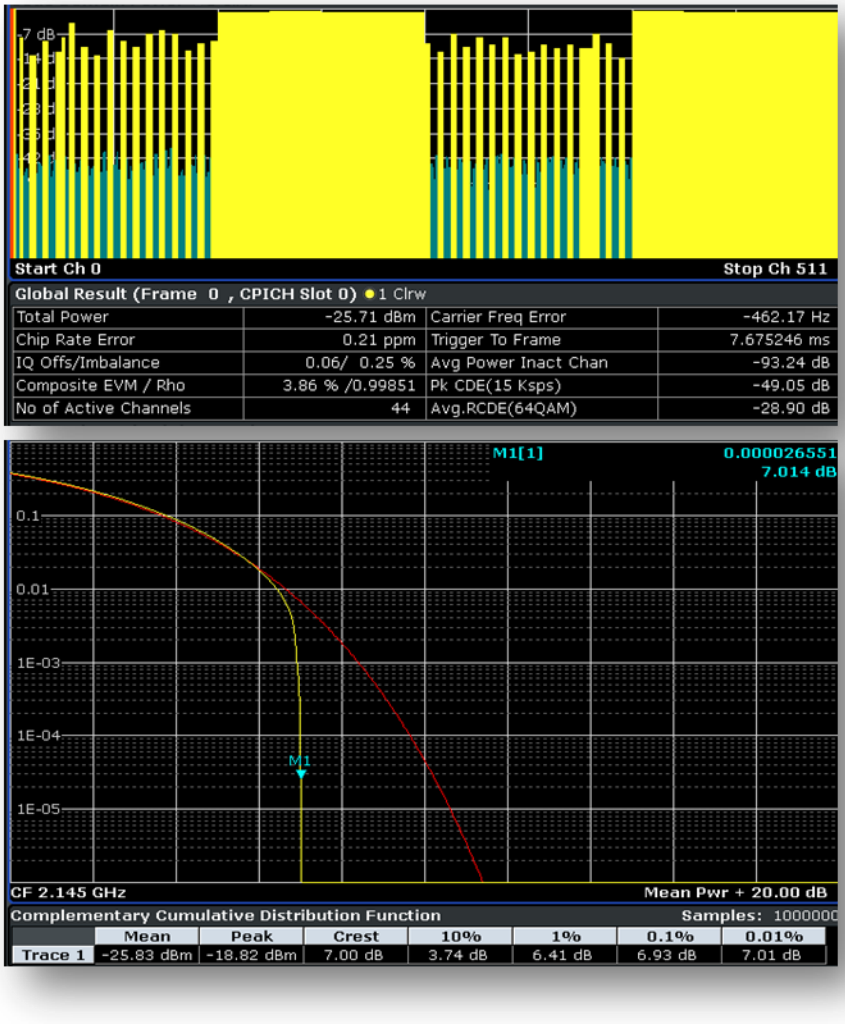
EXAMPLE

3GPP High Speed Downlink Packet Access (WCDMA)

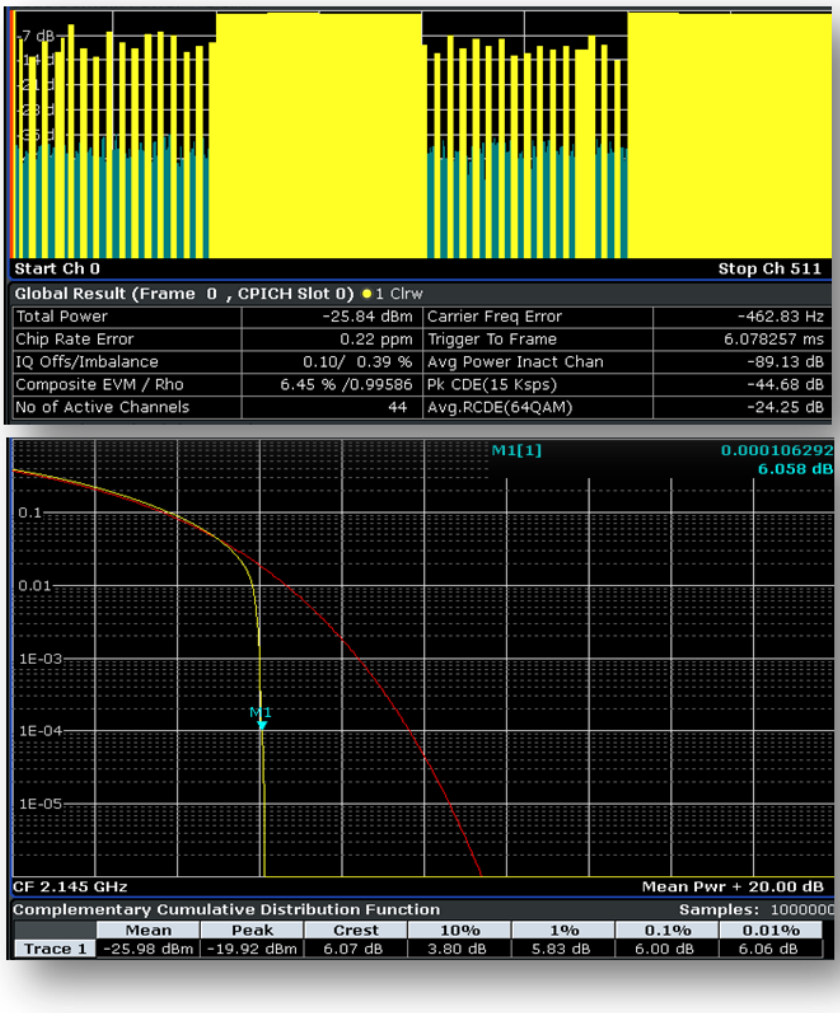
Measurement Information:

- Test measures performance with peak reduction to 7.0dB and 6.0dB against allowed 3GPP test parameters of EVM, PCDE and RCDE (64QAM).
- Test signal is 3GPP base station conformance Test Model 6 as specified by TS25.141 with 30x DPCH and 8x HS-PDSCH channels.
- Performance is measured at RF output of live test system with using Rhode & Swartz FSV Vector Signal Analyzer and WCDMA analysis software.

TM6-HSDPA-30+8: PAPR=7.0dB: EVM=**3.9%**, PCDE=-**49dB**, RCDE=**-28dB**



TM6-HSDPA-30+8: PAPR=6.0dB: EVM=**6.5%**, PCDE=**-43dB**, RCDE=-24dB



HSDPA – Performance Summary

MCPA WCDMA – TS25.141 TEST MODEL 6 - TM6-HSDPA-30+8					
Parameter	**3GPP Limit**	**Target**	**Measured**	**Target**	**Measured**
PAPR	N/A	7.0dB[1]	7.0dB[2]	6.0dB[1]	6.0dB[2]
EVM	17.5%	< 5.0%	3.9%	< 8.0%	6.5%
PCDE	-32dBc	< -37dBc	-49dBc	< -32dBc	-43dBc
RCDE	-20dBc	< -25dBc	-28dBc	< -20dBc	-24dBc

Table 1: 4CH WCDMA Measured Performance

Notes:

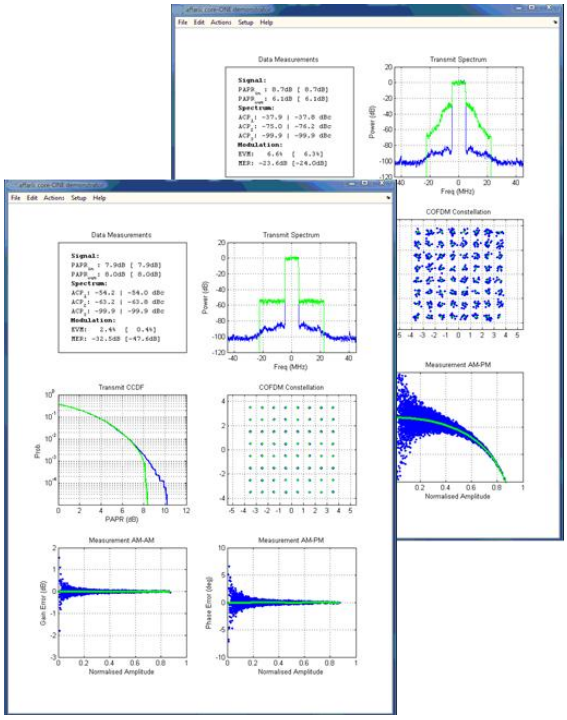
1. **PAPR reduction target as measured at output of CFR IP Core.**
2. **Measured at analyzer input with 40MHz measurement bandwidth.**

TOOL SUPPORT

The Crest Factor Processor core is supported with comprehensive PC based analysis tools to assist in core setup and performance analysis.

Analysis tools include FPGA frameworks for formal 3GPP conformance testing using MATLAB via USB based In Circuit Evaluation (ICE) tools.

Conformance test signal generation and analysis software complaint with 3GPP TS25.141 (WCDMA) and TS36.141 (LTE) are available for both development and production test environments.



PERFORMANCE

Table 2 summarises measured RF performance for the LLCFR block for WCDMA and LTE modulation with representative BTS hardware.

3GPP MEASURED RF PERFORMANCE – WCDMA (TS25.141) & LTE (TS36.141)			
Parameter	**PAPR**	**Measured EVM**	**3GPP EVM Limit**
WCDMA – HSDPA	7.0dB	3.9%	17.5%
LTE 20MHz - 64QAM	7.0dB	3.8%	12.0%

Table 2: 3GPP Measured RF Performance

These performance numbers include noise contributions of data conversion and mixing LO phase noise when measured with commercial test equipment.

For further performance information in different applications and configurations please contact sales@affarii.com.

AVAILABILITY

The DPD02 predistortion processor is available as a standalone IP block for Altera and Lattice FPGAs or as part of the digitalTRX solution set. For further information please contact sales@affarii.com

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